

10

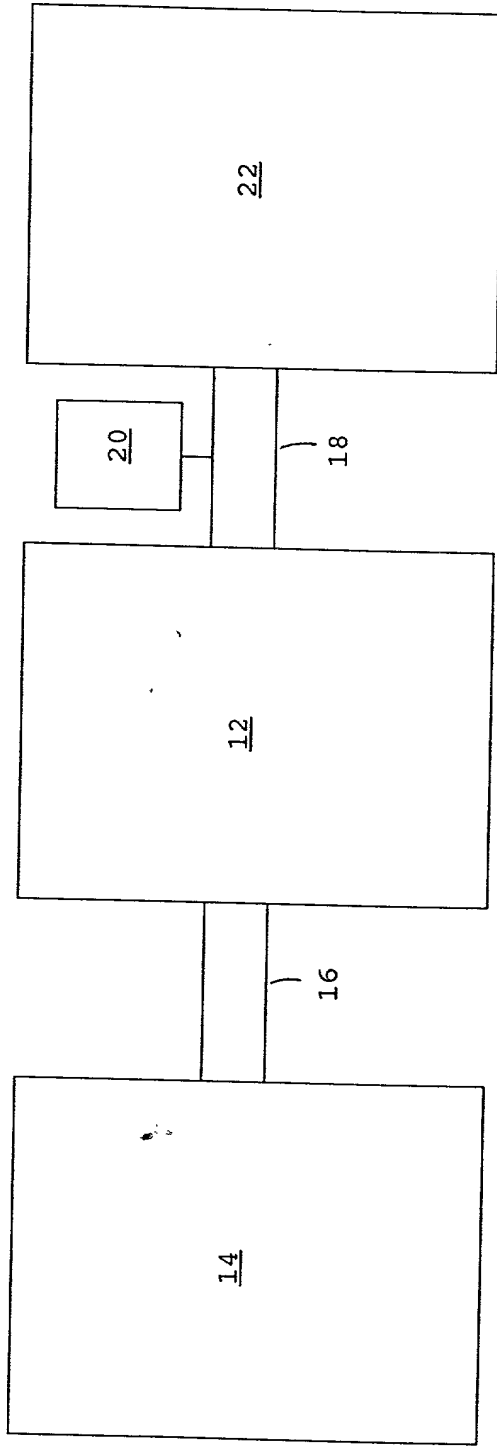
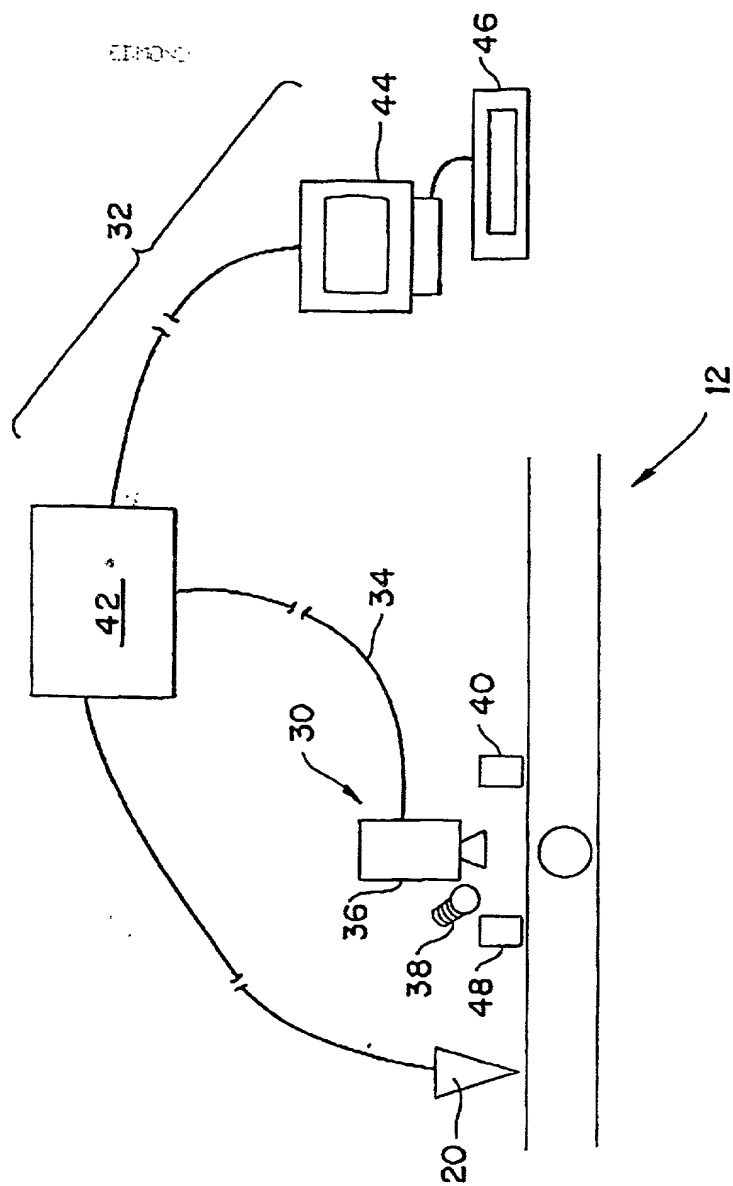


FIG. 1

FIG. 2



50

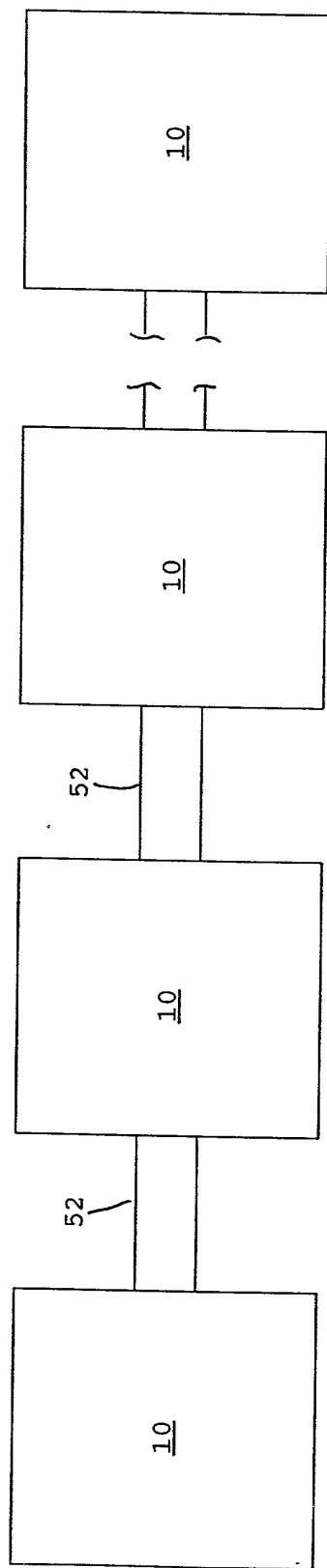


FIG. 3

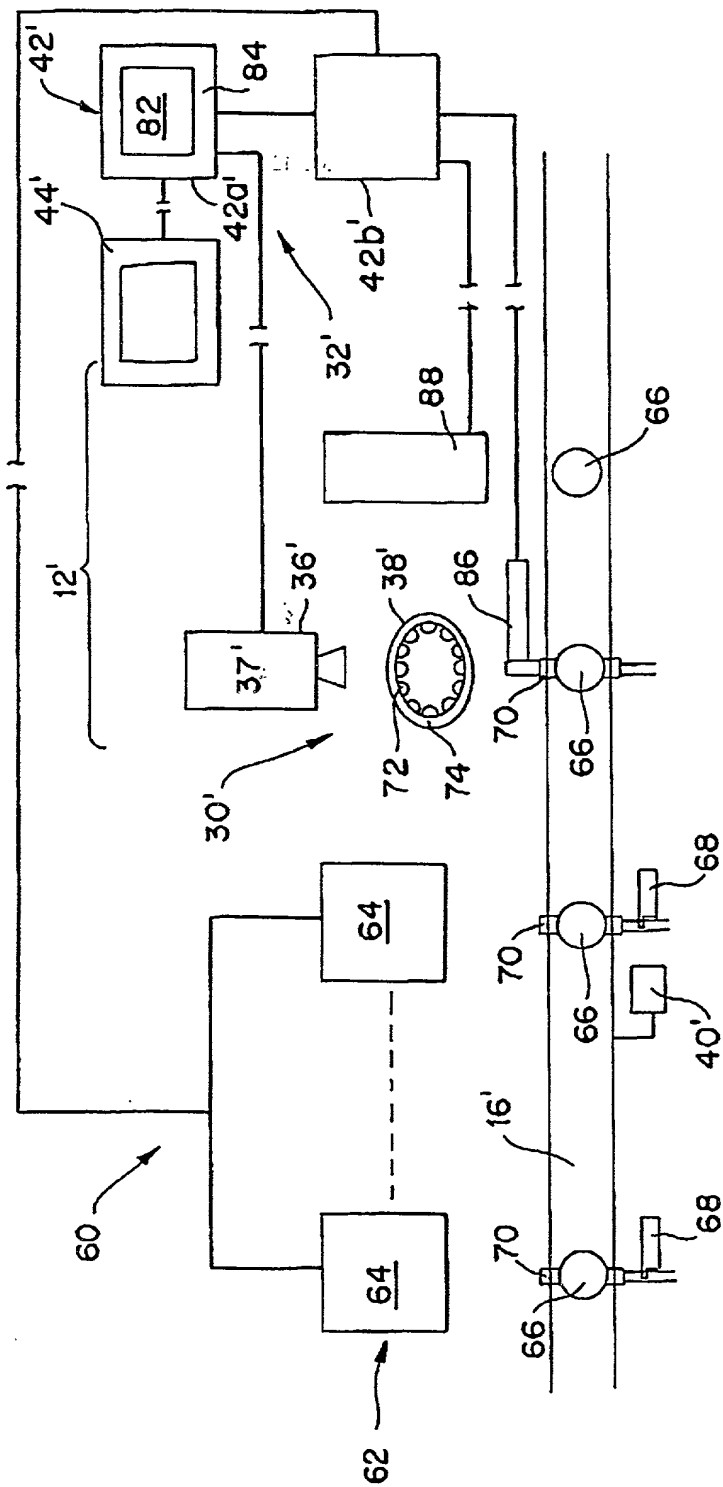
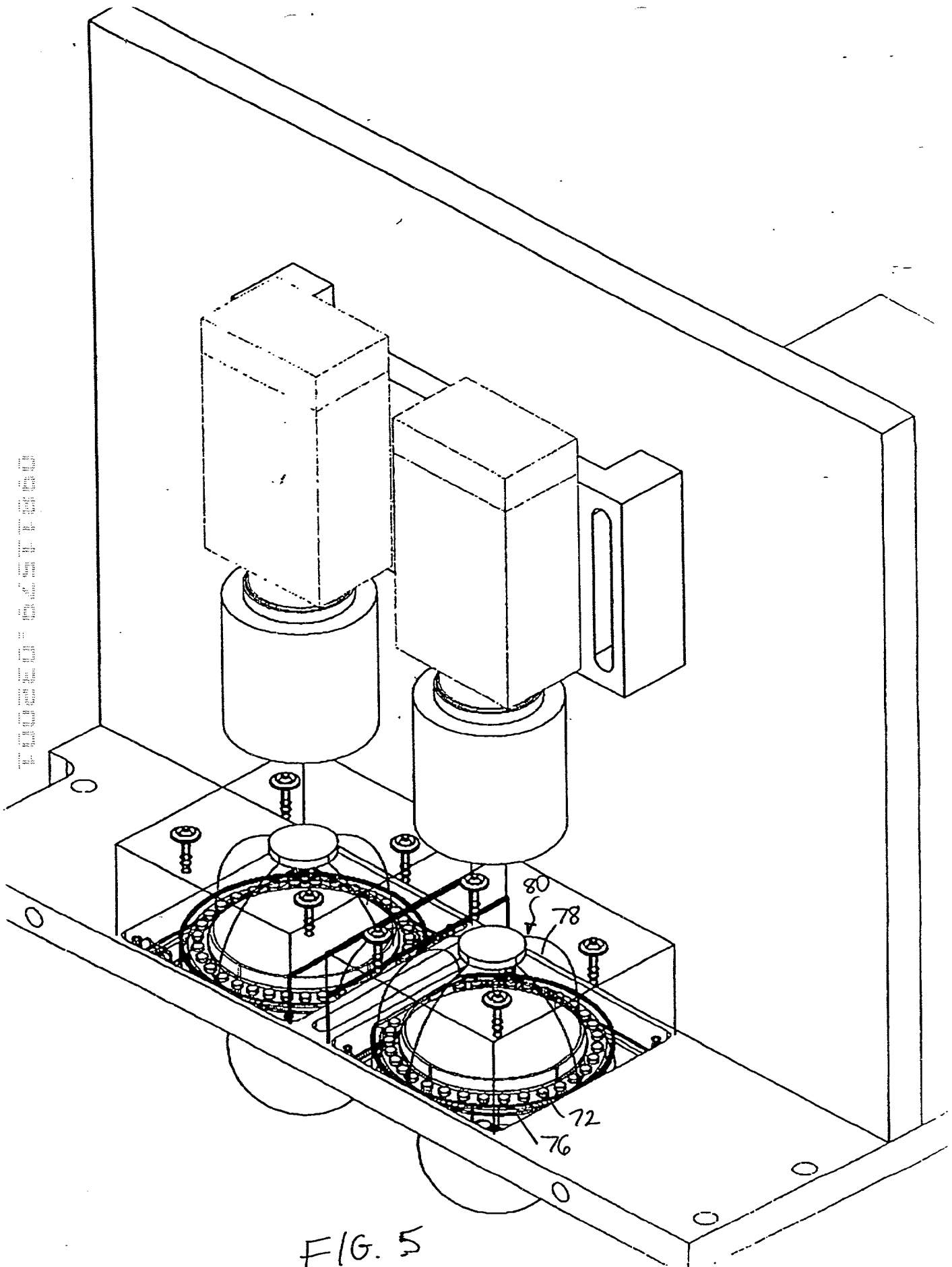


FIG. 4



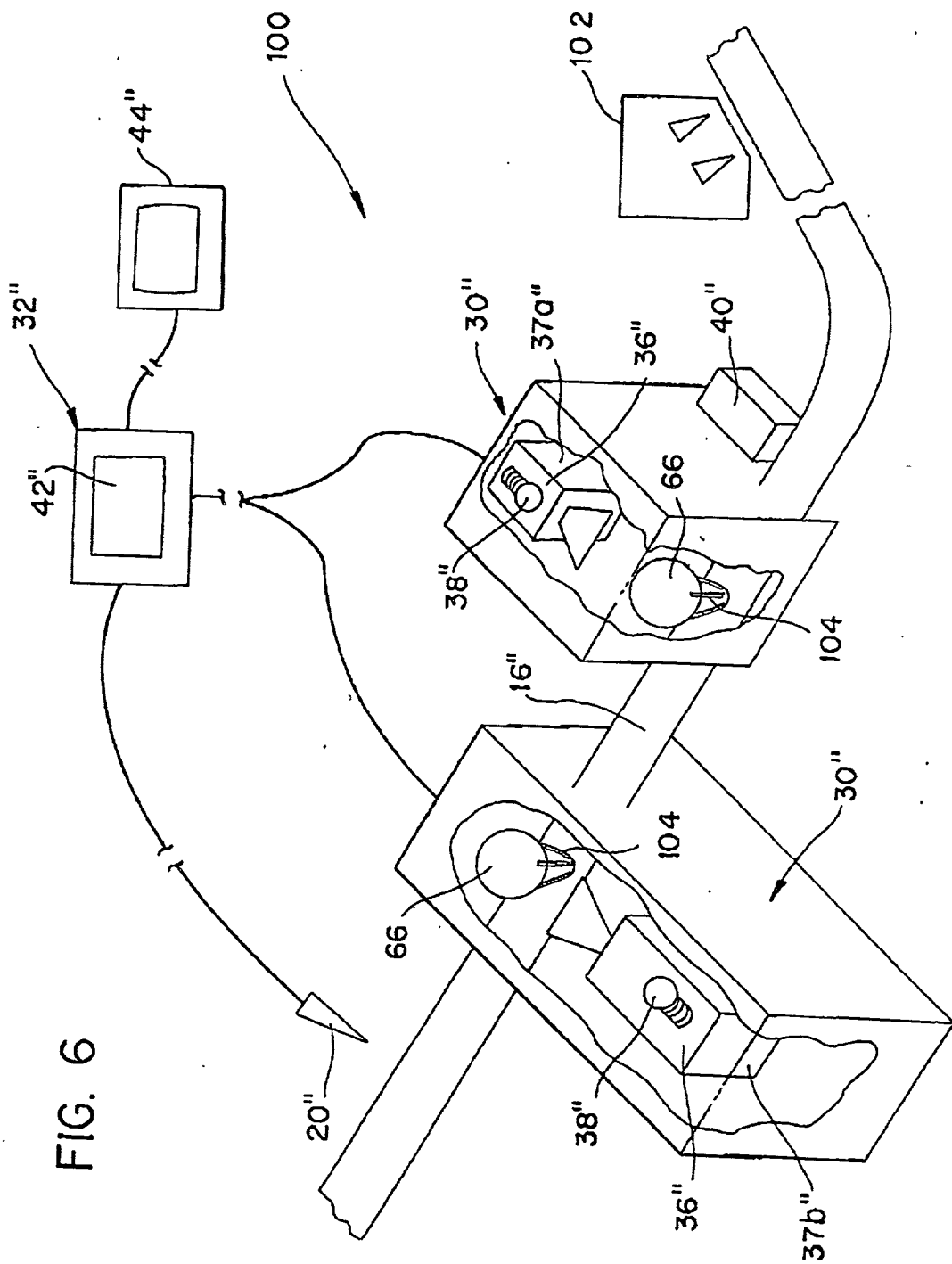


FIG. 7 is a block diagram of a system 120, which includes a processor 122, a memory 124, and a network interface 126. The processor 122 is connected to the memory 124 and the network interface 126. The memory 124 is connected to the network interface 126. The network interface 126 is connected to a network 128.

120

122

126

124

122

122

FIG. 7